Notice of Allowability	Application No.	Applicant(s)	
	10/801,808	HARS, LASZLO	
	Examiner	Art Unit	
	Michael Yaary	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *03/15/2004*.

2. ☒ The allowed claim(s) is/are *1-19*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20071119* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mark Wilson on 11/19/2007.

The examiner has amended the claims as follows:

- Replace the originally filed claims 1, 4, and 10, with amended claims 1, 4, and 10 below.

1. An apparatus for retaining maximum speed of a flip-flop metastability based random number generator, comprising:

a fixed delay unit having an input for receiving a common signal from a digital signal generator, said fixed delay unit providing a fixed period of delay to the signal as an output;

a variable delay unit having an input for receiving the common signal from the digital signal generator, said variable delay unit being tunable to provide a variable delay to the common signal as an output;

a pair of NAND gates each of which has a first input that receives a respective output of one of fixed delay unit and variable delay unit; an output of a first NAND gate

is input to a second NAND gate of the pair of NAND gates, and an output of the second NAND gate is input to the first NAND gate of the pair of gates;

a frequency measurement and delay tuning module that receives an output of a first NAND gate of the pair of NAND gates, said module checks the frequency of random number bit generation and updates the variable delay unit according to predetermined criteria to tune the variable delay unit so as to maximize the speed of the random bit generation.

4. The apparatus according to claim 2, wherein the frequency measurement and delay tuning module comprises a counter that is incremented each time a random bit is produced, and multiplied by a weight (<1) at every clock cycle and according to the following algorithm:

```
#define Weight 0.9990234375  //1-1/(2<<10)
Counter = Counter * Weight + IsRandomBitGenerated();.
```

10. A computer readable medium comprising the following algorithm of executable instructions, wherein the algorithm is used in tuning a variable delay unit using a frequency measurement and delay tuning module, when the algorithm of executable instructions is executed by a computer performs the following steps of:

(i) setting a queue length at a predetermined value;

(ii) setting a predetermined number of delay values;

(iii) designating a standard deviation (dmax) of steps;

(iv) starting with speed of 0;

(vi) setting an insertion point in the queue while keeping an infinite loop at maximum speed;

(vii) designating a number of steps of normal distribution;

(viii) ensuring that |step| > 0;

(ix) obtaining a last maximum speed and its index in the queue;

(x) setting the delay as imax;

(xi) repeating for next delay value (from 1 to 256);

(xii) setting delay (dly) and getting speed (spd);

(xiii) storing trial results of speed and updating a variable delay unit used for random number generation;

(xiv) moving/increasing insertion point I in the queue by 1;

(xv) if the insertion point i is > que length, and i = 1, then ending the routine;

(xvi) go to step (xi).

REASONS FOR ALLOWANCE

2. Claims 1-19 are allowed.

3. The following is an examiner's statement of reasons for allowance:

4. The prior art of record fails to teach or suggest the claimed invention. Specifically the prior art of record fails to teach or suggest a frequency measurement and delay tuning module that receives an output of a first NAND gate of the pair of NAND gates,

said module checks the frequency of random number bit generation and updates the variable delay unit according to predetermined criteria to tune the variable delay unit so as to maximize the speed of the random bit generation as taught by independent claim 1. The prior art of record fails to teach or suggest a computer readable medium comprising an algorithm of executable instructions, wherein the algorithm is used in tuning a variable delay unit using a frequency measurement and delay tuning module, when the algorithm of executable instructions is executed by a computer performs the steps as disclosed in independent claim 10. The prior art of record fails to teach or suggest adjusting the variable unit by a predetermined amount according to an algorithm that determines whether the variable delay should be larger, equal to, or smaller than optimum frequency by a predetermined amount based on the measured frequency of random bit generation, as disclosed in independent claim 15.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Pat. 3,947,697 - Synchronizing circuit including two flip-flops and circuit means to protect a synchronized signal from an unstable state of the flip-flops

US Pat. 4,929,850 – Metastable resistant flip-flop

US Pat. 5,343,414 – Apparatus for adaptively tuning to a received periodic signal

US Pat. 6,631,390 – Method and apparatus for generating random number using flip-flop meta-stability

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Yaary whose telephone number is (571) 270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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